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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/805,309	03/22/2004	Junichiro Kobayashi	SON-2977	9147

23353 7590 10/28/2005

RADER FISHMAN & GRAUER PLLC
LION BUILDING
1233 20TH STREET N.W., SUITE 501
WASHINGTON, DC 20036

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/805,309	KOBAYASHI, JUNICHIRO
	Examiner	Art Unit
	Thao X. Le	2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7 and 13-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7 and 13-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 03 Oct. 2005. These drawings are acceptable.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 13-15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by FR 2726125 to Delage et al.

Regarding claim 13, Delage discloses a semiconductor device in fig. 5b comprising: a semiconductor mesa portion (where emitter E is located) formed on a substrate including a stack of at least a collector layer (below cb layer), fig. 5b, a base layer cb, and an emitter layer E formed in narrower region compared with said base layer cb, fig. 5b, and functioning as an active region of a bipolar transistor; a base contact pad mesa portion R_B formed on said substrate apart from said semiconductor mesa portion (where E is located), fig. 1B, and formed with a height the same as the height of the top surface of said base layer cb, fig. 5b; and a conductive layer (Pont-a-air), fig. 5b, formed integrally with a base electrode (left portion of Pont-a-air in contact with base cb) formed connected to said base layer cb at part of a region of formation of

said base layer cb other than the region of formation of said emitter layer E, fig. 5b, a base contact pad electrode (right portion of Pont-a-air in contact with R_B) formed above said base contact pad mesa portion in a region other than near the edges of the top surface of said base contact pad mesa portion, fig. 5b, and an interconnect (middle portion of Pont-a-air) for connecting said base electrode and said base contact pad electrode, wherein said base electrode is formed in a region other than the region of formation of said emitter layer and other that near edges of said base layer, fig. 5b.

Regarding claim 14, Delage discloses a semiconductor device as set forth in claim 13, wherein the surface layer of said base contact pad mesa portion is formed by the same layer as said base layer cb, fig. 5b.

Regarding claim 15, Delage discloses a semiconductor device as set forth in claim 13, wherein the area under said conductive layer between said semiconductor mesa portion and said base contact pad mesa portion forms a space, fig. 5b.

Regarding claim 17, Delage discloses the semiconductor device as set forth in claim 1, wherein said semiconductor mesa portion is comprised of a stack of a compound semiconductor and has a heterojunction bipolar transistor, fig. 5b

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 5, and 7 rejected under 35 U.S.C. 102(e) as being anticipated by US 6870184 to Li et al.

Regarding claim 1, Li discloses a semiconductor device in fig. 4-12 comprising: a semiconductor mesa portion (middle portion) formed on a substrate 200, column 4 line 15, including a stack of at least a collector layer 204, a base layer 206, and an emitter layer 208, column 4 lines 14-16, formed in narrower region compared with said base layer 206, fig. 11, and functioning as an active region of a bipolar transistor; a base contact pad mesa portion 218, fig. 11, formed on said substrate 200 apart from said semiconductor mesa portion (middle portion) and formed with a height the same as the height of the top surface of said base layer 206, fig. 11; and a conductive layer 214, column 4 line 41, formed integrally with a base electrode (left portion of 214) formed connected to said base layer 206 at part of a region of formation of said base layer 206 other than the region of formation of said emitter layer 208, fig. 11, a base contact pad electrode (right portion of 214) formed above said base contact pad mesa portion 218 in a region other than near the edges of the top surface of said base contact pad mesa portion 218, fig. 11, and an interconnect (middle portion of 214) for connecting said base electrode and said base contact pad electrode, wherein an insulating film 224, fig. 11 col. 4 line 52 is formed below said conductive layer 214 between said semiconductor mesa portion (middle portion) and said base contact pad mesa 218 portion, fig. 11.

Regarding claim 2, Li discloses a semiconductor device as set forth in claim 1, wherein the surface layer of said base contact pad mesa portion 218 is formed by the same layer as said base layer 206.

Regarding claim 3, Li discloses a semiconductor device as set forth in claim 1, wherein the area under said conductive layer 214 between said semiconductor mesa portion and said base contact pad mesa portion forms a space.

Regarding claims 5, 7, Li discloses the semiconductor device as set forth in claim 1, wherein said base electrode is formed in a region other than the region of formation of said emitter layer 208 and other than near the edges of said base layer 206, fig. 11, wherein said semiconductor mesa portion is comprises a stack of a compound semiconductor and has a heterojunction bipolar transistor, see abstract.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-3,5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over by FR 2726125 to Delage et al. in view of US 6605825 to Brar et al.

Regarding claim 1, Delage discloses a semiconductor device in fig. 5b comprising: a semiconductor mesa portion (E/cb/B/C) formed on a substrate S, fig. 4, including a stack of at least a collector layer C, a base layer cb/B, and an emitter layer E

formed in narrower region compared with said base layer cb/B, fig. 5b, and functioning as an active region of a bipolar transistor; a base contact pad mesa portion R_B, fig. 5b, formed on said substrate S apart from said semiconductor mesa portion and formed with a height the same as the height of the top surface of said base layer cb/b, fig. 5b; and a conductive layer (Pont-air), formed integrally with a base electrode (left portion of Pont-a-air) formed connected to said base layer cb/B at part of a region of formation of said base layer cb/B other than the region of formation of said emitter layer E, fig. 5b, a base contact pad electrode (right portion of Pont-a-air) formed above said base contact pad mesa portion R_B in a region other than near the edges of the top surface of said base contact pad mesa portion R_B, fig. 5b, and an interconnect (middle portion of Pont-a-air) for connecting said base electrode and said base contact pad electrode.

But Delage does not discloses the semiconductor device wherein an insulating film is formed below said conductive layer between said semiconductor mesa portion and said base contact pad mesa portion.

However, Brar discloses the semiconductor device in fig. 8 wherein an insulating film 64, col. 6 line 2, is formed below said conductive layer 32, col. 3 lines 42 and 49, between said semiconductor mesa portion 10/12/14 and said base contact pad mesa portion (where 26 is located), fig. 8. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the insulating layer 64 teaching of Brar with Delage's method, because it would have provided the protection to the mesa layer and/or for further interconnection as taught by Brar in col. 6 lines 1-15.

Regarding claims 2-3 and 5-7 as discussed in the above claims 13-17, Delgae discloses all the limitations of claims 2-3, and 5-7.

8. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over by US6870184 to Li et al.

Regarding claim 6, Li does not disclose the semiconductor device as set forth in claim 1, wherein a distance between said semiconductor mesa portion and said base contact pad mesa portion is 1 to 5 micron.

However, Li discloses a general distance or a gap between said semiconductor mesa portion and said base contact pad mesa portion, fig. 5b. Accordingly, it would have been obvious to one of ordinary skill in art to use general gap teaching of Li in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

9. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over by FR 2726125 to Delage et al.

Regarding claim 16, Delage does not disclose the semiconductor device as set forth in claim 1, wherein a distance between said semiconductor mesa portion and said base contact pad mesa portion is 1 to 5 micron.

However, Delage discloses a general distance or a gap between said semiconductor mesa portion and said base contact pad mesa portion, fig. 5b. Accordingly, it would have been obvious to one of ordinary skill in art to use

general gap teaching of Delage in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Response to Arguments

10. Applicant's arguments with respect to claims 1-3,5-7 and 13-17 have been considered but are moot in view of the new ground(s) of rejection.

11. With respect to Li, Applicant cannot rely upon the foreign priority papers to overcome this rejection because a translation of said papers has not been made of record in accordance with 37 CFR 1.55. See MPEP § 201.15.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
Patent Examiner
17 Oct. 2005

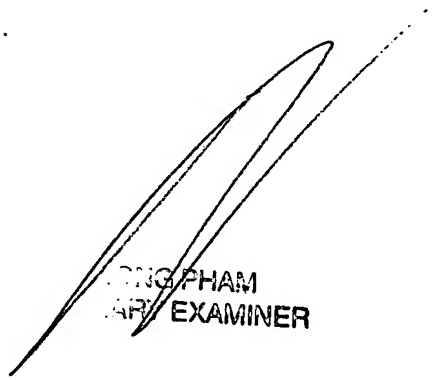
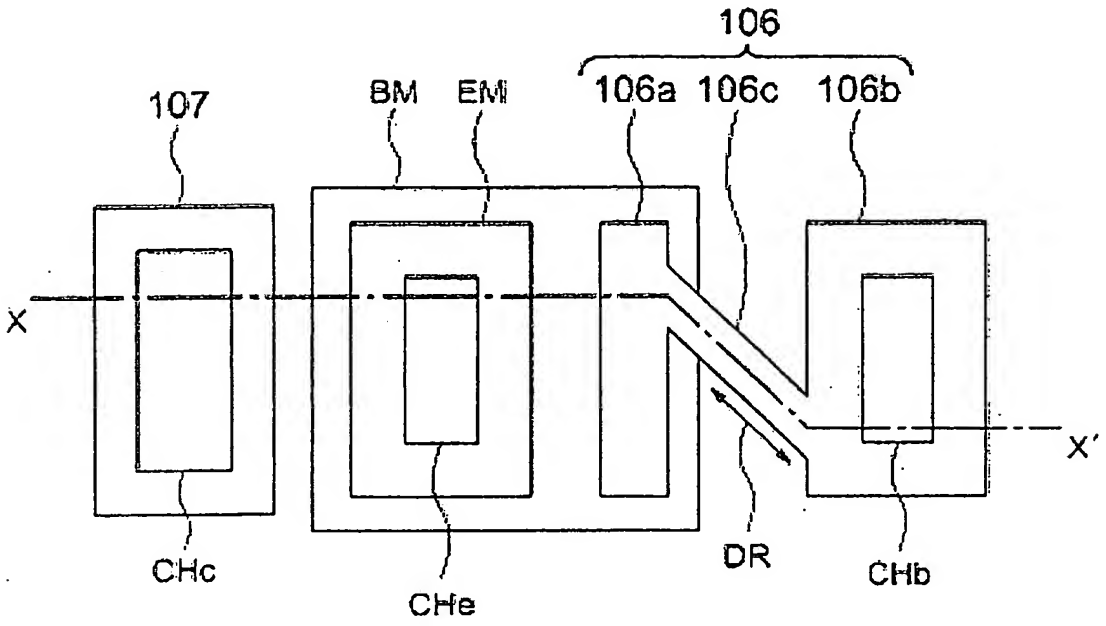


FIG. 1A PRIOR ART



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PRIOR ART FIG. 1B

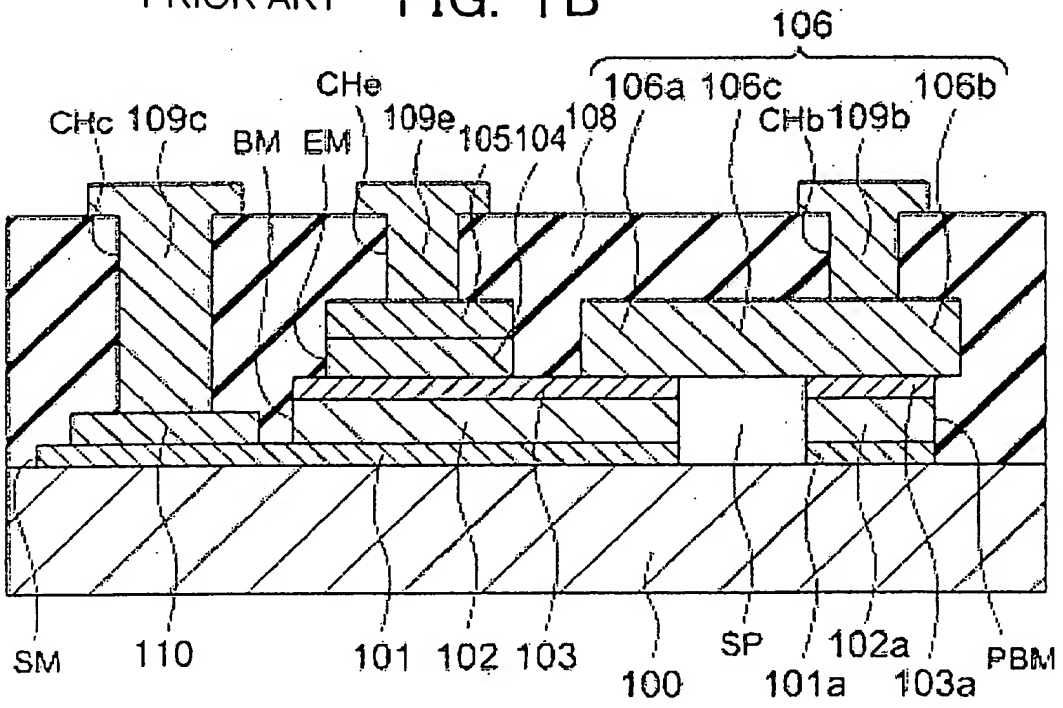


FIG. 2A PRIOR ART

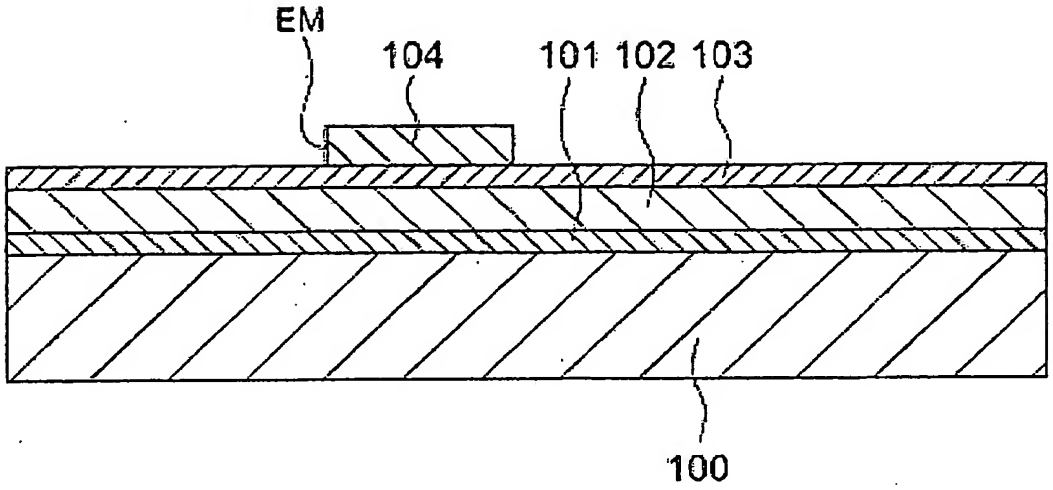


FIG. 2B PRIOR ART

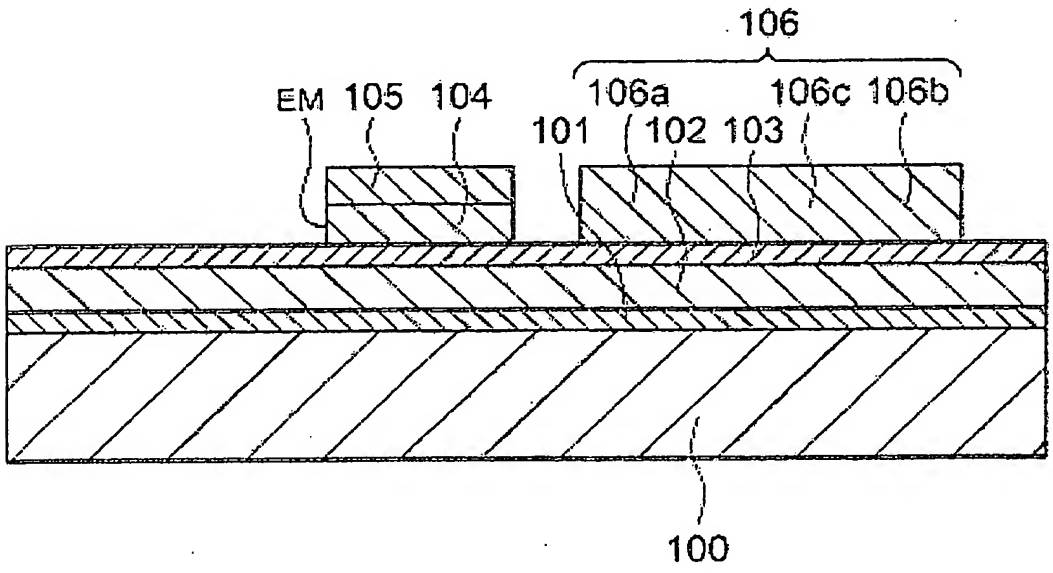
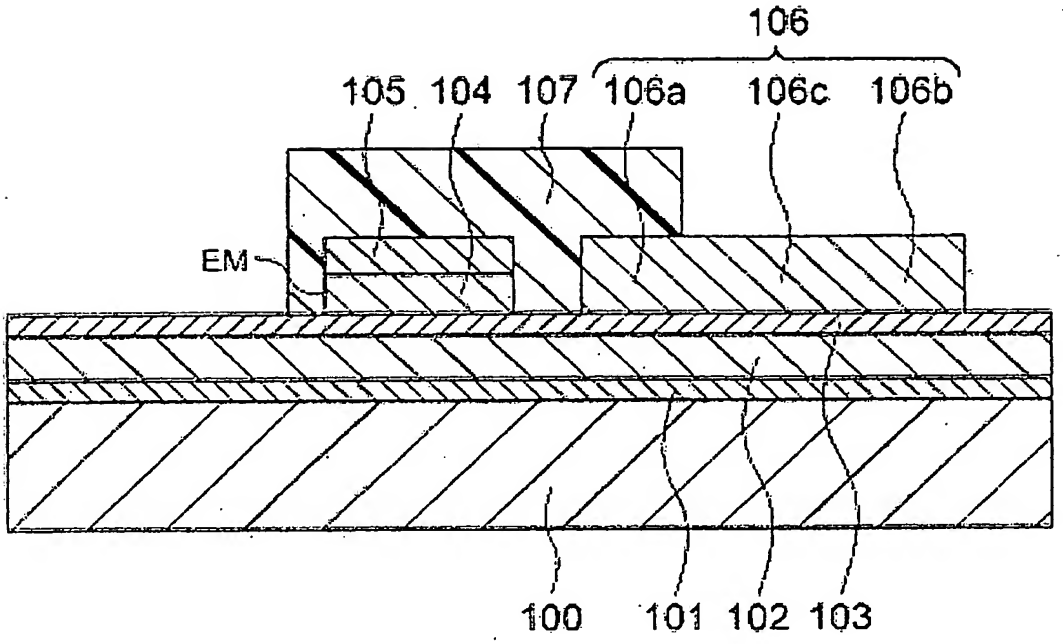


FIG. 2C PRIOR ART



PRIOR ART FIG. 2D

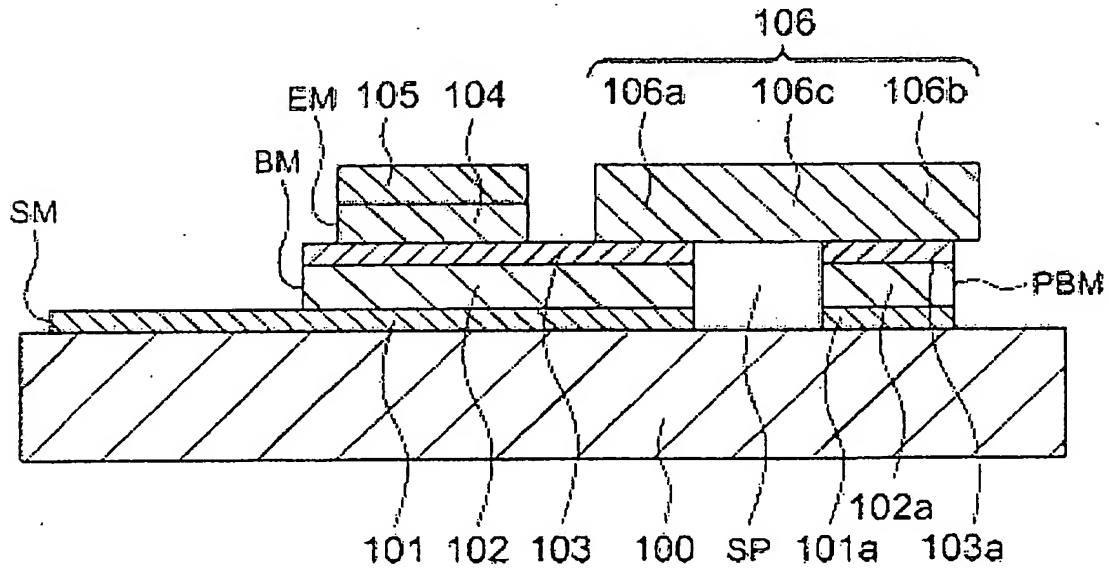


FIG. 3A

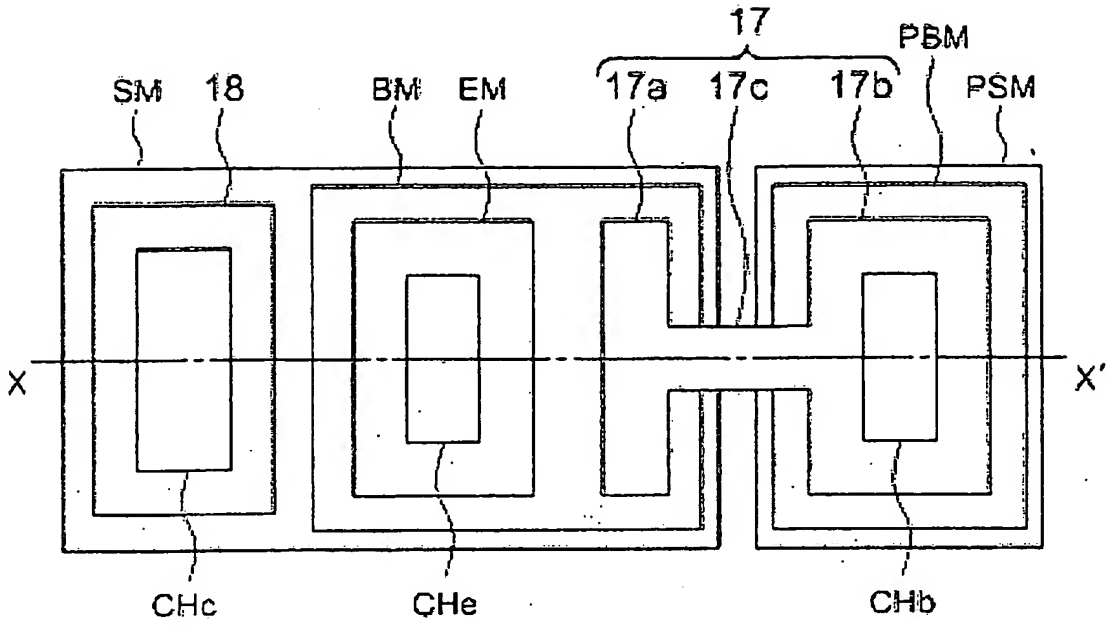


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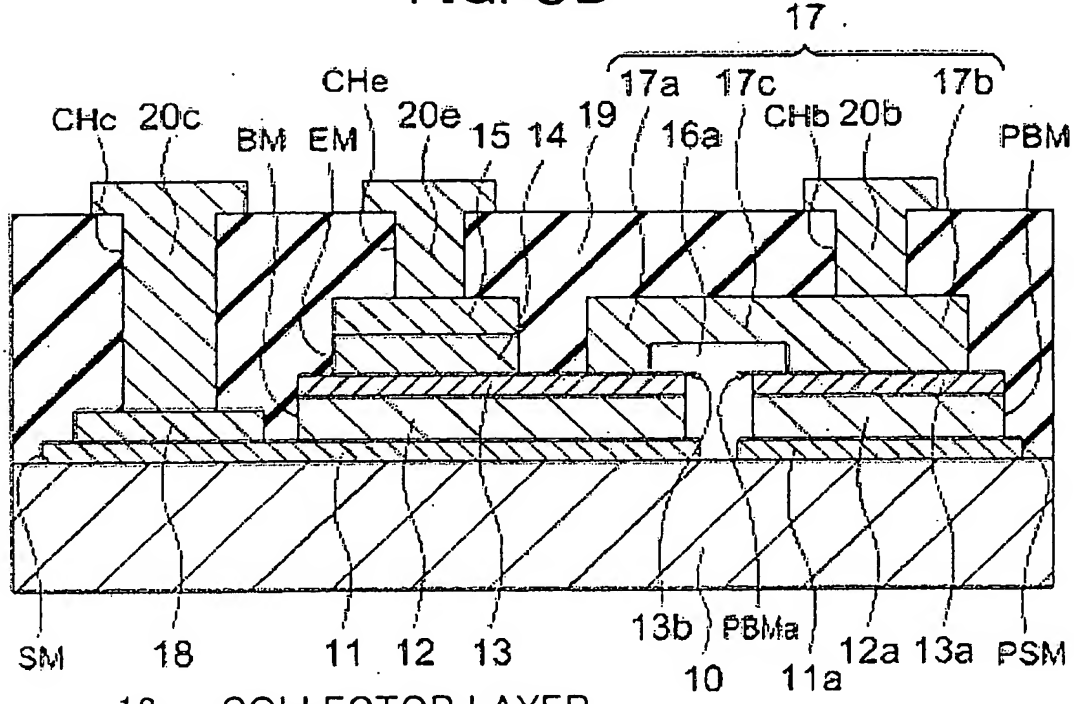
FIG. 3B



12···COLLECTOR LAYER
13···BASE LAYER
14···EMITTER LAYER
17···INTERCONNECTING LAYER
17a···BASE ELECTRODE
17b···BASE CONTACT PAD ELECTRODE
17c···INTERCONNECTING PORTION
PBM···BASE MESA STRUCTURE FOR USING BASE CONTACT PAD